Modified GDI Technique - A Power Efficient Method For Digital Circuit Design

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Abstract- This paper presents logic style comparisons based on different logic functions and claimed modified Gate Diffusion Input logic (Mod-GDI) to be much more power-efficient than Gate Diffusion Input logic (GDI) and complementary CMOS logic design. However, DC and Transient analysis performed on more efficient modified Gate Diffusion Input logic (Mod-GDI) circuit realizations and a wider range of different logic cells, as well as the use of practical circuit arrangements reveal Mod-GDI to be superior to GDI and CMOS in the majority cases with respect to speed, area, power dissipation, and power-delay products. This manuscript shows that Mod-GDI is the logic style of preference for the realization of arbitrary combinational circuits, if low voltage, low power, and small power-delay products are of concern. All Simulations are performed through PSPICE based on 0.18 \( \mu \)m CMOS technology, and results show power characteristics of Mod-GDI technique of low power digital circuit design. Simulation results shows up to 45% reduction in power-delay product in Mod-GDI. This technique is appropriate for designing of fast, low power circuits, using reduced number of transistor (as compared to CMOS techniques), while improving power characteristics.

Keywords – Low power, Power minimization, Ultra low power VLSI circuits, Logic style, CMOS, GDI, Mod-GDI, and Logic gates, AND, OR, MUX, digital circuits, DC analysis, transient response.

I. INTRODUCTION

Among the forceful investigation in the field of low power, high speed digital applications due to the growing demand of systems like phones, laptop, palmtop computers, cellular phones[1], wireless modems and portable multimedia applications etc has directed the VLSI technology to scale down to nano-regimes, allowing additional functionality to be incorporated on a single chip[2]. The designer’s novel purpose in the field of multifaceted digital circuit design is minimization of power consumption [3]. These investigations are responsible for special design techniques for digital circuits distant from conventional CMOS design style. A large body of investigate has been performed to expand and advance conventional Complementary Metal Oxide Semiconductor (CMOS) techniques for the fabrication of ULTRA low power integrated circuits (ICs)[4]. The purpose of this study is to expand a faster, lower power, and reduced area substitute to standard CMOS logic circuits. Mod-GDI technique is one such new technique for minimization of power consumption in the digital circuit design field [5].

II. MODIFIED GATE DIFFUSION INPUT LOGIC STYLE (Mod-GDI)

Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental constraint in order to get better the performance of [6] a variety of low power and high performance devices. Morgenshtein et al. investigated a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI).[7] with reduced area and power necessities, and proficient of implementing a broad variety of logic functions. FIG. 1 shows basic GDI logic cell, which is used for implementing verity of logic functions and circuits at low power and high speed design where G, P and N are three inputs and output is taken from D terminal. Table 1 represents the logic functions which can be implemented with the help of this basic GDI cell [1,2]. But this basic Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic style [4,5].
Table 1: Various Logic Functions Implemented with of Basic GDI Cell

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>D</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>B</td>
<td>A</td>
<td>A'B</td>
<td>F1</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>High</td>
<td>A</td>
<td>A' + B</td>
</tr>
<tr>
<td>High</td>
<td>B</td>
<td>A</td>
<td>A+B</td>
<td>OR</td>
</tr>
<tr>
<td>B</td>
<td>Low</td>
<td>A</td>
<td>AB</td>
<td>AND</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>A'B</td>
<td>MUX</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
<td>A</td>
<td>A'</td>
<td>NOT</td>
</tr>
</tbody>
</table>

Table 2: Various Logic Functions Implemented with of Mod-GDI Cell

<table>
<thead>
<tr>
<th>N</th>
<th>S_N</th>
<th>P</th>
<th>S_P</th>
<th>G</th>
<th>D</th>
<th>FUNCTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>A</td>
<td>A'</td>
<td>1</td>
<td>INVERTER</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A</td>
<td>A-B</td>
<td>B</td>
<td>1</td>
<td>AND</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A</td>
<td>A-B</td>
<td>B</td>
<td>1</td>
<td>OR</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>A'B</td>
<td>A'</td>
<td>1</td>
<td>XOR</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>A'B</td>
<td>1</td>
<td>XNOR</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>1</td>
<td>MUX</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>A+B</td>
<td>1</td>
<td>FUNCTION 1</td>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>A'B</td>
<td>1</td>
<td>FUNCTION 2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>1</td>
<td>MUX</td>
</tr>
</tbody>
</table>

A. Advantages of Mod-GDI:

This uncomplicated arrangement as shown in Fig 2 has made the fabrication of GDI cells compatible with the standard nano-scale CMOS fabrication process. Whereas many leakage components can be recognized in sophisticated sub-micron technologies, the most important leakage currents are given below [9]:

1. Sub-Threshold Leakage, 2. Gate Leakage (caused by electron tunneling)

This exceptional arrangement of Mod-GDI cell provides considerable reduction of both sub-threshold and gate leakage compared to static CMOS gate. These methodologies may be used as a basis for efficient synthesizer implementation, to achieve area efficient designs such as: Reduction of Short-Circuit Current, Repeaters etc which make this logic style exceptionally appropriate for low power and high speed applications.

B. Important Features of Mod-GDI Technique In Brief:

a. The Mod-GDI logic style provides a low-power and area efficient substitute to existing logic styles, which is implementable in all current CMOS transistor fabrication technologies. Mod-GDI is appropriate for design of high-speed, low power circuits, using reduced number of transistors, even as improving swing degradation and static power dissipation.
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power characteristics, and allowing easy top-down design by using a small cell library. Mod-GDI is appropriate for implementation of a broad range of logic circuits, using a variety of transistor technologies. Mod-GDI logic style performance is testable; so that Mod-GDI logic style and logic circuit design methods is therefore a promising new approach to logic circuit design.

b. Realization of logic functions in Silicon-on-Insulator (SOI) or Silicon-on-Sapphire (SOS) fabrication technologies presents considerable reduction of wires used for interconnect, in these methods, the floating bulk transistors are frequently used for logical circuit’s implementations for GDI logic style and for other existing logic styles. Floating bulk transistors not requires connections of the $V_{DD}$ and GND wires to the transistors bulks. Consequently, when a logic function is implemented with Mod-GDI cells with SOI or SOS transistors, $V_{DD}$ and GND interconnect wires are not required because the Mod-GDI cell requires $V_{DD}$ and GND only to supply the bulks. This is in contrast to the majority previous design methodologies which would still need $V_{DD}$ and GND to supply the circuits [10].

III. DC & TRANSIENT ANALYSIS OF FUNCTIONS USING MODIFIED GDI TECHNIQUE

This section presents implementation of basic logic functions using modified gate diffusion input technique. This is a power efficient method for digital circuit design, which is very important for VLSI design. This technique is superior to CMOS and GDI logic style in terms of power dissipation and no. of transistors used for logic circuit designing. So here, an analysis is done and all logic functions are verified with the help of DC and Transient analysis. Based on the results power delay is calculated for Mod-GDI logic style and compared with the CMOS logic style, which shows that Mod-GDI logic style is more beneficial for lower power digital design.

A. Implementation of Mod-GDI ‘OR’ Function

When input $G = A$, $P = B$, $S_P = D$, $N = VDD$ [1 or High], and $S_N = 0$, then output $D = A+B$ which is OR function. Fig 3 shows input configuration for Mod-GDI OR Fn, where; At Node ‘1’ input $G = A$ is given, At Node ‘2’ input $P = B$ is given, At Node ‘3’ output $D = A+B$ is taken, At Node ‘4’ input $N = VDD$ [1 or High] is given. Truth table for DC analysis is shown which satisfied the logic OR function implemented with Mod-GDI logic style.

\[ \begin{array}{c|c|c|c|c|c} 
 G & P & S_P & N & S_N & D \\
 \hline 
 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 1 & 0 & 0 & 0 & 1 \\
 1 & 0 & 0 & 0 & 0 & 1 \\
 1 & 1 & 0 & 0 & 0 & 1 \\
 \end{array} \]

ii) Transient O/P of Mod-GDI ‘OR’ Function:

Figure 4 shows the transient analysis of Mod-GDI OR function. Here V(1) is input voltage at G, V(2) is input voltage at P, and V(3) is output voltage at D as shown in figure 3. Fig. 4 shows V(3) is high when any one input of V(1) and V(2) is at high level and V(3) is low only when both inputs V(1) and V(2) is at low levels which satisfied the logic OR function implemented with Mod-GDI logic style. This analysis is done with setting the V(2) at zero level and then varying V(1) and V(3) is analyzed.
B. Implementation of Mod-GDI ‘AND’ Function

When input \( G = A, N = B, P = 0, S_P = VDD \) [1 or High], and \( S_N = 0 \), then output \( D = A \cdot B \) which is AND function.

Fig 5 shows input configuration for Mod-GDI AND Fn, where; At Node ‘1’ input \( G = A \) is given, At Node ‘2’ input \( N = B \) is given, At Node ‘3’ output \( D = A \cdot B \) is taken, At Node ‘4’ input \( P = 0 \) is given. Truth table for DC analysis is shown which satisfied the logic AND function implemented with Mod-GDI logic style.

Fig 5: Mod-GDI ‘AND’ Fn

\[
\begin{array}{cccccc}
\text{Input} & G & N & S_P & S_N & D & \text{output} \\
\hline
0 & 0 & 0 & 0 & 0 & VDD & 0 \ [0.000000 V] \\
0 & 0 & 1 & 0 & 0 & VDD & 0 \ [0.000005 V] \\
1 & 0 & 0 & 0 & 0 & VDD & 0 \ [0.000000002 V] \\
1 & 1 & 0 & 0 & 0 & VDD & 1 \ [3.552 V] \\
\end{array}
\]

\( i) \) DC Analysis; Truth Table:

\( ii) \) Transient O/P of Mod-GDI ‘AND’ Function:

Figure 6 shows the transient analysis of Mod-GDI AND function. Here \( V(1) \) is input voltage at \( G \), \( V(2) \) is input voltage at \( N \), and \( V(3) \) is output voltage at \( D \) as shown in figure 5. Fig.6 shows \( V(3) \) is high only when both input of \( V(1) \) and \( V(2) \) is at high level and \( V(3) \) is low when anyone of both inputs \( V(1) \) and \( V(2) \) is at low levels which satisfied the logic AND function implemented with Mod-GDI logic style. This analysis is done with setting the \( V(2) \) at high level and then varying \( V(1) \) and \( V(3) \) is analyzed.
C. Implementation of Mod-GDI ‘F1’ Function

When input $G = A$, $N = 0$, $P = B$, $S_P = VDD$ [1 or High], and $S_N = 0$, then output $D = \bar{A}B$ which is F1 function. Fig 7 shows input configuration for Mod-GDI F1 Fn, where; At Node ‘1’ input $G = A$ is given, At Node ‘2’ input $P = B$ is given, At Node ‘3’ output $D = \bar{A}B$ is taken, At Node ‘4’ input $S_P = VDD$ is given. Truth table for DC analysis is shown which satisfied the logic F1 function implemented with Mod-GDI logic style.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|}
\hline
Input & Output  \\
\hline
$G = A$ & $P = B$ & $S_P$ & $S_N$ & $D$ & $\bar{A}B$ [F1 Fn] \\
0 [0V] & 0 [0V] & VDD & 0 & 0 & 0 [0.000005 V] \\
0 [0V] & 1 [5V] & VDD & 0 & 0 & 1 [4.99 V] \\
1 [5V] & 0 [0V] & VDD & 0 & 0 & 0 [0.000000002 V] \\
1 [5V] & 1 [5V] & VDD & 0 & 0 & 0 [0.000000002 V] \\
\hline
\end{tabular}
\caption{Mod-GDI ‘F1’ Function Truth Table}
\end{table}

ii) Transient O/P of Mod-GDI ‘F1’ FUNCTION:

Figure 8 shows the transient analysis of Mod-GDI F1 function. Here V(1) is input voltage at G, V(2) is input voltage at P, and V(3) is output voltage at D as shown in figure 7. Fig.8 shows V(3) is high only when V(1) input is at low level and V(2) is at high level and V(3) is low otherwise which satisfied the logic F1 function implemented with Mod-GDI logic style. This analysis is done with varying the both inputs V(1) and V(2) at low and high level and then V(3) is analyzed.
D. Implementation of Mod-GDI ‘F2’ Function

When input G = A, N = B, P = 1, S\textsubscript{P} = VDD [1 or High], and S\textsubscript{N} = 0, then output D = \bar{A} + B which is F2 function. Fig 9 shows input configuration for Mod-GDI F2 Fn, where; At Node ‘1’ input G = A is given, At Node ‘2’ input N = B is given, At Node ‘3’ output D = \bar{A} + B is taken, At Node ‘4’ input P = 1 is given. Truth table for DC analysis is shown which satisfied the logic F2 function implemented with Mod-GDI logic style.

ii) Transient O/P of Mod-GDI ‘F2’ Function:

Figure 10 shows the transient analysis of Mod-GDI F2 function. Here V(1) is input voltage at G, V(2) is input voltage at N, and V(3) is output voltage at D as shown in figure 9. Fig 10 shows V(3) is high only when input V(1) is at high level and V(2) may be either at high or at low level. The output V(3) varying according to the input V(1).
E. Implementation of Mod-GDI ‘MUX’ Function

Fig 11 shows MUX function using Mod-GDI technique. When input $G = A$, $N = C$, $P = B$, $S_P = VDD$ [1 or High], and $S_N = 0$, then output $D = \overline{A}B + AC$ which is MUX function. Fig 11 shows input configuration for Mod-GDI MUX Fn, where; At Node ‘1’ input $G = A$ is given, At Node ‘2’ input $P = B$ is given, At Node ‘3’ output $N = C$ is given, At Node ‘4’ input $S_P = VDD$ is given. At Node ‘5’ output $D = \overline{A}B + AC$ is taken. Truth table for DC analysis is shown which satisfied the logic MUX function implemented with Mod-GDI logic style.

$$\begin{array}{c|c|c|c|c|c} 
\text{Input} & \text{Output} \\
\hline 
G = A & P = B & S_P & N = C & S_N & D = \overline{A}B + AC; \text{[MUX Fn]} \\
0 \{0V\} & 0 \{0V\} & VDD & 0 \{0V\} & 0 & 0 \{0.0000005\ V\} \\
0 \{0V\} & 0 \{0V\} & VDD & 1 \{5V\} & 0 & 0 \{0.0000005\ V\} \\
0 \{0V\} & 1 \{5V\} & VDD & 0 \{0V\} & 0 & 1 \{4.99\ V\} \\
0 \{0V\} & 1 \{5V\} & VDD & 1 \{5V\} & 0 & 1 \{4.99\ V\} \\
1 \{5V\} & 0 \{0V\} & VDD & 0 \{0V\} & 0 & 0 \{0.0000000002\ V\} \\
1 \{5V\} & 0 \{0V\} & VDD & 1 \{5V\} & 0 & 1 \{3.552\ V\} \\
1 \{5V\} & 1 \{5V\} & VDD & 0 \{0V\} & 0 & 0 \{0.0000000002\ V\} \\
1 \{5V\} & 1 \{5V\} & VDD & 1 \{5V\} & 0 & 0 \{3.552\ V\} \\
\end{array}$$

Fig 10: Mod-GDI ‘F2’ Fn Transient Response

ii) Transient O/P of Mod-GDI ‘MUX’ Function:

Figure 12 shows the transient analysis of Mod-GDI F1 function. Here $V(1)$ is input voltage at $G$, $V(2)$ is input voltage at $P$, and $V(3)$ is input voltage at $P$ and $V(5)$ is output voltage at $D$ as shown in figure 11.
Fig 12: Mod-GDI ‘MUX’ Fn Transient Response

F. Implementation of Mod-GDI ‘Inverter’ Function
When input \(G = A, N = 0, P = 1, S_P = VDD\) [1 or High], and \(S_N = 0\), then output \(D = \bar{A}\) which is INVERTER function. Fig 13 shows input configuration for Mod-GDI INVERTER Fn, where; At Node ‘1’ input \(G = A\) is given, At Node ‘2’ input \(P = 1\) is given, At Node ‘3’ output \(D = \bar{A}\) is taken. Truth table for DC analysis is shown which satisfied the logic Inverter function implemented with Mod-GDI logic style.

\[
\begin{array}{c|c|c|c|c|c|c}
\text{Input} & G = A & P = 1 & S_P & S_N & D = \bar{A}; \text{[Inverter Fn]} \\
\hline
0 & 0 & 1 & 0 & 0 & 1 \\
1 & 5 & 1 & 0 & 0 & 0 \\
\end{array}
\]

Fig 13: Mod-GDI ‘Inverter’ Fn

\(i)\) Dc Analysis; Truth Table:

\(ii)\) Transient O/P Of Mod-GDI ‘Inverter’ Function:
Figure 14 shows the transient analysis of Mod-GDI INVERTER function. Here \(V(1)\) is input voltage at \(G\) and \(V(3)\) is output voltage at \(D\) as shown in figure 13. Fig 14 shows \(V(3)\) is at high level only when \(V(1)\) is at low level which shows the inverter function of input signal. When input is at low level, output is high and when input is at high level, output is low.
The simulation and performance analysis is done using PSPICE based on 0.18μm CMOS technology. The basis logic functions are simulated using Mod-GDI logic style. The performance analysis of Mod-GDI and CMOS logic is presented in this table 3. The performance evaluation is made with respect to the switching delay, transistor count and power consumed by Mod-GDI and CMOS logic. From the analysis it is observed that the Mod-GDI performance is better when comparing to CMOS logic. In CMOS the number of transistors used to realize a function is twice that of Mod-GDI. The power consumed by CMOS is slightly higher than Mod-GDI. It is observed that Mod-GDI logic style has low area, low power and low delay when compared to CMOS logic style.

<table>
<thead>
<tr>
<th>Function</th>
<th>Logic Expression</th>
<th>MOD-GDI LOGIC</th>
<th>CMOS LOGIC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Power (µw)</td>
<td>Delay (ns)</td>
</tr>
<tr>
<td>OR</td>
<td>A+B</td>
<td>17.80</td>
<td>1.01</td>
</tr>
<tr>
<td>AND</td>
<td>A'B</td>
<td>17.90</td>
<td>1.10</td>
</tr>
<tr>
<td>F1</td>
<td>A'+B</td>
<td>25.00</td>
<td>1.59</td>
</tr>
<tr>
<td>F2</td>
<td>A'+B</td>
<td>25.00</td>
<td>0.40</td>
</tr>
<tr>
<td>MUX</td>
<td>A'B+AC</td>
<td>25.00</td>
<td>0.50</td>
</tr>
</tbody>
</table>

The comparison between our analysis and prior works indicates that one of this logic styles for low power digital design does provide many advantages. In short, the proposed Mod-GDI logic style based designs can be taken a better alternative in future. For the period of the desktop PC design and portable age VLSI design efforts have paying attention primarily on optimizing speed to realize computationally intensive real-time functions such as video compression, gaming, graphics etc. As a result, semiconductor ICs that successfully integrated a variety of complexes signal processing modules and graphical processing units to meet up computation and entertainment demands. As these solutions have addressed the real-time problem, they have not addressed the increasing demand.
for portable operation, where mobile phone needs to pack all this without consuming much power. The severe limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements. At the same time as wireless devices are quickly making their way to the consumer electronics market, a key design restriction for portable operation that is the total power consumption of the device must be taken into account. So for this purpose reducing the total power consumption in such systems is significant because it is advantageous to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries. Consequently the most significant issue to consider while designing portable devices is 'low power design' for which a Mod-GDI logic style is proposed.

V. CONCLUSION

In this paper an approach is presented for minimizing power consumption for digital circuits at the logic style level and DC and Transient analysis of basic logic gates has been done using Mod-GDI logic style. All Simulations are performed through PSPICE based on 0.18μm CMOS technology, and results show power characteristics of Mod-GDI technique of low power digital circuit design. Simulation results shows up to 45% reduction in power-delay product in Mod-GDI. Mod-GDI approach allows realization of a broad variety of multifaceted logic functions by means of only two transistors. Mod-GDI gates lower the transistor count and in turn the silicon area required when compared to standard static CMOS and Domino CMOS based approaches. The leakage power and switching power of Mod-GDI gates is lower than the traditional logic styles. The problem of fabrication of GDI gates in standard nano-scale CMOS process is overcome by connecting the sources of pMOS and nMOS to VDD and GND respectively in Mod-GDI logic style. The problem of threshold drop is not a very serious issue in deep sub-nm regions. The Mod-GDI logic style based design adopts interruption of inverter to alleviate the problem of signal degradation during propagation. This proposed logic style is analyzed to exploit the high speed potential and low power feature of Mod-GDI based circuit applications. The comparison between our analysis and prior works indicates that one of this logic styles for low power digital design does provide many advantages. In short, the proposed Mod-GDI logic style based designs can be taken a better alternative in future.

V. REFERENCE

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