CMOS current comparator with Regenerative property

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Abstract— In recent years, there have been major advances in CMOS VLSI technology, which generated great interest in electronic circuits, which is more efficient by perfection performance and power consumption. Circuits, called multi valued logic circuits offer several potential opportunities for improvement of present vlsi designs. Current mode CMOS multivalued logic circuits are interesting and have many applications in wireless communications. This paper shows the CMOS multi valued current comparator design and to obtain precise output using regenerative property.

Index Terms— multi valued logic, current comparator, current mirror, power dissipation, regenerative property

I. INTRODUCTION

The comparator circuit provides an output by comparing input signal to reference signal. The operation of analog circuit are now a days is done by impressing current as an input in place of voltage as a input signal. The voltage comparator has several disadvantages such as higher power dissipation, offset voltage, and operation frequency etc. The current as an input in place of voltage in circuit, the better performance can be achieved due to some advantages of current source like low $V_{dd}$ requirement, less sensitive to noise disturbance, high speed and lower power dissipation. In CMOS VLSI devices current mode operations have been considered as an alternative in analog circuit designs. Comparators are used in many applications like data converters, other front end signal processing applications. In current comparator the current comparison done by impressing the current pulse signal as an input of the comparator .The comparator finds whether it is negative of positive. The comparator circuit provides the output is used properly to indicate the result of operation.

As voltage-mode ADCs already operate at maximum potential and further improvements are difficult due to the limitations of the active elements. The current-mode ADCs have a potential possibility to improve the parameters by introducing new circuit solutions. Current comparators are basic building blocks for nonlinear current-mode signal processing and analogue to digital converters. The desired features of a current comparator include high speed, low input impedance, low power and low supply voltage. Among these requirements, the speed for low current levels is very critical in many situations since it can be the limiting factor of the overall speed of a system. For instance, the speed of a current-mode A/D converter is limited by the response time of the comparator at its minimum input current levels for a given possibility of meta-stability error.

Digital binary systems use just two logic symbols, “0” and “1” to represent all information. Since the real world is not binary, we cannot surely claim that using two values is an optimum choice. Multiple-valued circuits can be realized as voltage-mode or current-mode, depending on the operation and complexity of the circuit. On voltage-mode circuits, the information is transferred by voltage levels. Ternary circuits are better candidates for voltage-mode realization, especially for the circuits using dual supply voltages and signed digit arithmetic. Maximum allowable radix of the voltage-mode designs are determined by the supply voltage. As the technology developed, chip densities have increased and only very little power can be dissipated per cell to avoid the chip from overheating. That makes supply voltage levels critical in circuit designs. In addition, for portable electronic devices, battery life is directly related to power consumption, which makes low power design very important criteria for analog and digital integrated circuits. Since power consumption of the circuit is related to the square of the supply voltage, reduction of the supply voltage is the first choice for reducing power consumption, leading into reducing
dynamic range of the voltage-mode signal. As a result, we have limited radix at voltage-mode. Using transistors having variable threshold voltages can be thought as a solution for voltage mode designs but it is still limited with quaternary logic levels. The proposed circuit in [3] proposes a low input impedance current comparator using pulse width modulation technique which is useful in wireless communications. The comparator circuit design with low power and high speed are proposed by [4] compared to [7]. After well design are proposed by [5], [6] with high speed.

On current-mode realizations of multiple-valued logic circuits, the information is transferred by current levels, that are integer multiples of a reference current. Current-mode circuits allow higher radix than voltage-mode circuits, which makes them preferable to voltage-mode ones as we need to increase the system speed and the information content of the current carrying wires. The main advantage of the current-mode multi-valued circuits is the simplicity of the addition operation. This basic and most used operation of logic design can be performed simply by connecting signal lines into a single node, resulting in a reduced number of active devices in the circuit. Every single addition operation in binary logic design requires 20 transistors. In addition, currents can be copied, scaled and algebraically sign-changed with a simple current mirror. However, current-mode circuits have larger static power consumption and unlike binary circuits, they are not self-restoring. Cascaded stages will result a deviation from the predefined output levels, and it is necessary to restore the output to its original level.

II. CURRENT MIRROR

Fig1 shows a basic current mirror circuit with nmos transistor

![Current Mirror Circuit](image)

\[ I_{\text{in}} = I_{\text{ref}} \frac{1}{2} \beta \frac{W}{L} (V_G - V_{\text{TN}})^2 \]  

(1)

If \( V_G \) is applied to another transistor

\[ V_G = \sqrt{\frac{I_{\text{ref}}}{\beta \frac{W}{L}}} + V_{\text{TN}} \]  

(2)

\[ I_{\text{out}} = \frac{I_{\text{ref}}}{2} \frac{W}{L} \]  

(3)

Mirror circuits are used to produce the replicas of input currents. They can be designed as n-type or p-type as shown in Figure2. These circuits are used to provide fan-out greater than one, because current-mode CMOS logic allows fan-out of only one.

In addition, by rearranging transistor dimensions, any current value in the design can be multiplied by a constant \( k \) (called the scale factor), as shown in Figure3 and their direction (sign)
CMOS current comparator with Regenerative property

![Fig2: nmos and pmos current mirror](image1)

III. Current comparator

The circuit introduced in Figure 6 is the simplest form of current-comparator circuits. Input diode-connected NMOS-PMOS transistor pair produces the threshold current. When the drain and gate of a MOSFET are connected together the result is a two-terminal device known as a diode-connected transistor. Using an active load, i.e., MOSFET(s), to replace a passive load resistor can dramatically reduce the required chip area for the circuit while also helping produce much higher gains (due to the potentially high small-signal resistance an active load can provide). An active load can be implemented using a gate-drain connected (a.k.a. diode-connected) MOSFET or a current source/sink. This reference current is mirrored to output as I_{th}, and input current is mirrored to output as I_{in}. The output of the comparator circuit is at logical HIGH voltage (output node has the same potential with power supply) when the input current is less than the threshold current and at logical LOW voltage (output node has the same voltage with the ground) when the input current is greater than the threshold current as shown in Equation. Applying the input current over PMOS transistor mirror, and threshold current over NMOS, produces the inverted version of output voltages, if needed.

\[
V_o = \begin{cases} 
\text{High} & \text{if } I_{in} < I_{th} \\
\text{Low} & \text{if } I_{in} \geq I_{th} 
\end{cases}
\]  

(4)
IV. MULTIVALUED CURRENT COMPARATOR

In the Multi valued circuit,[1] have nmos and pmos current comparators. We are neglecting channel length modulation so Wilson current mirror[2] in CMOS current comparator is not needed. The comparator is made up of diode connected input nmos transistor M2 and nmos transistor M8, M9 and M910 to replicate this input current. A reference current is generated by pair transistors M1 and M2 and pmos transistors M2, M7 and M8 are used to replicate the reference current, the circuit configuration act as the reference current source. As the comparator switches current in the input $I_{IN}$ the input nmos current mirror transistor pairs M7, M8, M9 AND M10 will try to replicate the input current at its drain. The comparator output can be seen at the drains of transistors M8, M9 and M910 as logic high when the input current is less than the threshold current and logic low when the input current is higher than the source current. Another way to describe the circuit is to consider it is current mirror that reproduces current $I_{IN}$ as $I_{d8}$, $I_{d9}$ and $I_{d10}$ and then drives a high impedance active load to covert the current difference to an output voltage.
By applying current pulse as input output wave is generated.

We are getting appropriate transient response \[2\] but \(V_{\text{min}} = 1.37V\) for output at C when implemented which is more than the threshold voltage for most of the vlsi components.

V. PROPOSED CIRCUIT
In the proposed circuit we have added two inverters in series at each output as shown in Fig 7. A gate with regenerative property ensure that a disturbed signal converges back to a nominal voltage level we use inverter at the output.
CMOS current comparator with Regenerative property

Fig 10: Implementation of proposed circuit

Fig 11: Desired output (Vout (max) =5v and Vout (min)=0v)

We have obtained $V_{\text{min}} = 8\text{mV}$ which is desirable
VI. CONCLUSION

CMOS current comparator circuit, with precise output has been obtained. Since the need of faster and more low power devices is crucial factor for compact electronic design, multi-valued cmos current comparators provides a reliable option which have the advantages and can be used in both digital and analogue domains efficiently.

REFERENCES


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