CMOS dynamic low pass filter for a low noise level and a fast response time of PLL system

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Abstract—We present in this paper a new model of a low pass filter (LPF) for a Phase-Locked Loop (PLL) systems. The main characteristic of this CMOS LPF structure is its dynamic band-width (about 12.66kHz when the PLL is locked and 211.30kHz during the tracking). It ensures a fast response time, a suppression of the jitters and a better noise level at the output. This LPF polarization is ensured by the current from the PFC-IC (Phase-Frequency Comparator with Charge Impulse) and the VCO control voltage. The simulation in a PLL system gives us a response time of 35.4 µs and a phase noise level of -121.37dBc. Significant improvements could be expected with a dedicated CMOS process and design.

Keywords—CMOS, cut-off frequency, dynamic LPF, fast response time, jitters, locking, PFC-IC, PLL system, tracking.

I. INTRODUCTION

The PLL is largely used in communication systems such as Ethernet and wireless RF systems for fast data transmission. These systems require a very low jitter and a very short response time, a micro scale (even nano) integration, especially with the fast increase of the operating frequency [1, 2, 3]. Some solutions based on adjustable band-width [4] have improved the response time, and some based on ferroelectric capacitor [5] have reduced the oscillator jitter and thus the phase noise.

It should be noted that the response time and the phase noise depend on the cut-off frequency; indeed, for a narrow band width we can obtain a very low phase noise but a long response time and for a large band width, we can obtain a very short response time but a high phase noise level. To avoid this trade-off, in [4], the authors propose to change the LPF band-width with the PLL state (locked or not) and use in [6] the reference signal as a part of the VCO control voltage.

The circuit brought in [4] has a response time of 100µs; it musts probably also take higher surface for integration. For the Current-Mode PLL solution, in spite of the good response time (50ns) and relatively good noise level (- 74 dBc) during the locking PLL state, this systems is very sensitive to the fluctuations of the DC sources because of the inductances used in the loop filter and in the CCO (Current Controlled Oscillator) [1].

In this paper, we propose a new solution based on a dynamic LPF. Firstly, we describe and calculate a classical PLL system. Secondly, we focus on the new model of a LPF with dynamic CMOS resistance. Finally, we present simulation results of a PLL system working with that CMOS LPF.
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II. PLL SYSTEM

A PLL system is a physical device which reproduces at its output, the image of its input phase signal. Fig.1 is an example of PLL block diagram of which the fundamental elements are the phase-frequency comparator (PFC), the low pass filter (LPF), a voltage controlled oscillator (VCO) and a frequency divider (DF).

This PLL system is described by (1), (2) and (3).

\[ G(s)H(s) = \frac{K_{PFC}K_{VCO}F(s)}{Ns} \]  \hspace{1cm} (1)

\[ G(s) = \frac{K_{PFC}K_{VCO}F(s)}{s} \]  \hspace{1cm} (2)

\[ H(s) = \frac{1}{N} \]  \hspace{1cm} (3)

Where \( G(s) \) is the forward loop gain, \( H(s) \) is a reverse loop gain and \( G(s)H(s) \) is the open loop transfer function of the PLL. \( K_{PFC} \) expressed in [volt/radian] or in [amp/radian] (in the case of a PFC-IC) is the gain of the PFC in; \( K_{VCO} \) expressed in [hertz/volt] is the VCO gain and \( N \) is the divider ratio. \( F(s) \) is the low pass filter transfer function.

We consider for our system the second order LPF shown in the Fig.2 below where \( i_p \) is the output current from the PFC-IC and \( v_c \) is the VCO control voltage.

The calculation of the transfer function \( F(s) \) for this filter gives us:

\[ F(s) = \frac{1 + \tau_1 s}{s[CT(1 + \tau_2 s) + C2(1 + \tau_1 s)]} \]  \hspace{1cm} (4)

With \( \tau_1 = R1C1 \) and \( \tau_2 = R2C2 \) the time-constants; \( s \) is the Laplace variable. From relations (1) and (4), we deduce the following open loop transfer function of the system

\[ G(s)H(s) = \frac{Kv(1 + \tau_1 s)}{s^2[CT(1 + \tau_2 s) + C2(1 + \tau_1 s)]} \]  \hspace{1cm} (5)
Where \( \text{Kv} = \frac{K_{pdc} K_{v(H)}}{N} \), subsequently we define \( \tau_3 = \frac{C_2 \tau_1 + C_1 \tau_2}{C_1 + C_2} \).

In the frequency domain, \( s = j\omega \) and (5) becomes

\[
G(j\omega)H(j\omega) = -\frac{\text{Kv}}{\omega^2(1 + \tau_1 j\omega)(1 + \tau_3 j\omega)}
\]

From (6) we deduce the phase expression given by (7).

\[
\phi(\omega) = \tan^{-1}(\omega_3) - \tan^{-1}(\omega_{13}) - 180^\circ
\]

The cut-off frequency is the frequency of unity loop gain for maximum phase margin; his expression is given by (8).

\[
\omega_c = \frac{1}{\tau_1 \tau_3}
\]

A MATLAB simulation of Fig.3 shows that the cut-off frequency varies from 12.66kHz to 211.3kHz for \( 0.1\Omega \leq R_2 \leq 1\Omega \), considering \( C_1=4nF, R_1=3.5K \) and \( C_2=0.5pF \) found after calculation and optimization.

Fig.3: Cut-off frequency \( \omega_c \) as a function of the resistance \( R_2 \) of the LPF

The simulation above and the calculations reveal that changing the cut-off frequency from 12.66 kHz to 211.3k Hz will change the phase margin from 86.78° to 63.2° which is the acceptable phase margin.

Thus, the objectives of fast response time and low phase noise level can both be achieve if \( R_2 \) takes different values during tracking (in the order of the kilo Ohms) and once locked (in the order of the mega Ohms).

This can be achieved with MOS transistors which exhibit between the drain and the source, a resistance which can vary from a few hundreds of Ohm to a mega Ohm, depending on its polarization voltages.
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III. NEW MODEL OF A LPF WITH DYNAMIC CMOS RESISTANCE

(a): LPF with its CMOS structure

(b): LPF with R2_MOS equivalent resistance of the CMOS structure

Fig.4: New model of a LPF

A. Operational principle

According to the Fig. 4-(a),

\[ v_{c1} - v_c = V_{ds} = V_{gs} \] (9)

This, for each of the n characteristics \( I_{ds} = f(V_{ds}) \) gives us for each of the two CMOS transistors when conducting

\[ v_{c1} - v_c = V_{ds} = (V_{gs})_n \] (10)

Here, \((V_{gs})_n\) represents the voltage \( V_{gs} \) of the nth characteristic \( I_{ds} = f(V_{ds}) \), i.e. the value \((V_{gs})_n = \text{Constant}\) .

According to [7], we have

\[ f(V_{ds}) = \frac{K_n W_n}{\ell} \left( V_{gs} V_{ds} - \frac{V_{ds}^2}{2} \right) \] (11)

Where \( V_{gt} = V_{gs} - V_{Th} \); \( K_n \), \( W_n \) and \( \ell \) are defined according to the CMOS process.

In the case of the PMOS, \( K_n \) and \( V_{Th} \) will be quite simply replaced by \( K_p \) and \( V_{Tp} \), for resulting to similar formulas; \( V_{Th} \) and \( V_{Tp} \) represent the threshold voltages of the NMOS and the PMOS respectively. For two perfectly complementary CMOS transistors, we have

\[ |V_{Tp}| = V_{Th} = V_T \]

The conductance 1/R2_MOS is thus the variable slope of the following function

\[ I_{ds} = f(V_{ds} = (V_{gs})_n) \] (12)

The diagram in Fig.5 shows the simulation curve of \( I_{ds} \) with a variable slope. These CMOS transistor models are from Spice and the simulation is made with ADS (Advanced Design System).

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Fig. 5: CMOS characteristic $I_{DS} = f(V_{DS} = (V_{GS}))$; $IDS$ in Ampere (A) and $VDS$ in Volt (V).

- **Locking**
  When the system is locked $I_p = 0$ and $V_{TP} < V_{GS} < V_{TN}$. The two CMOS transistors are said to be blocked.
  If $|V_{TP}| = V_{TN} = V_T$, then we will have $-V_T < V_{GS} < V_T$.
  
  $I_{DS} \rightarrow 0$ and $|V_{cl} - V_c| = |I_{DS}| =$ constant $< V_T$
  
  $\frac{dI_{DS}}{dV_{DS}} = \frac{dI_{DS}}{d(V_{cl} - V_c)} = \frac{1}{R_{2\_MOS}} \rightarrow 0$

Fig. 4-(a) can therefore be simplified as shown in Fig. 6 below.

![Fig. 6: Equivalent diagram of the dynamic LPF in the locking state](image)

According to Fig. 6, we can derive the following expression where $r = R_{1} + R_{2\_MOS}$

$v_c = v_{c1} - rI_{DS}$

$I_{DS} \rightarrow 0$ imply $r = R_{1} + R_{2\_MOS} \rightarrow \infty (= 10^6 \Omega)$.

Hence, we have $v_c = $ constant; this corresponds to a perfect voltage source, thus ensuring a complete suppression of the jitters and therefore a very good output level of noise.
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• Tracking
After a locking PLL system limit, i.e. \(|V_{gs}| = V_T\), we have
\[ |v_c - v_{cl}| = |V_{ds}| = (|V_{gs}| > |V_T|) \] (15)

Two cases are to be distinguished:

* \(v_{cl} - v_c = (V_{gs})_o > 0\) (or \(f_{in} > f_{out}\); \(f_{in}\) and \(f_{out}\) are respectively the input and the output PLL systems frequencies): in this case, the NMOS is conducting and the PMOS blocked.

* \(v_{cl} - v_c = (V_{gs})_o < 0\) (or \(f_{in} < f_{out}\)): here, the PMOS is conducting and the NMOS blocked.

B. General expression of the conductance \(1/R\) of the CMOS transistor pair.

The Drain current in a NMOS transistor is given by (16) [7, 8]
\[ I_{ds} = \frac{KnWn}{1} \left( V_{GT} V_{ds} - \frac{V_{ds}^2}{2} \right) \] (16)

For \(V_{ds} \gg V_{gt}\) we have the following relation [8]
\[ I_{ds} = \frac{KnWn}{1} \left( V_{GT}^2 \right) \] (17)

For \(V_{ds} \ll V_{gt}\) we have the following relation [7]
\[ I_{ds} = \frac{KnWn}{1} V_{GT} V_{ds} \] (18)

According to (18), for small values of \(V_{ds}\) (CMOS transistor in ohmic zone operation), the transistor behaves like a dynamic resistance and thus, we have the following relation.
\[ I_{ds} = (1/R) V_{ds} \] (19)

In equation (19), the conductance \(1/R\) satisfies the following relation [7, 8]:
\[ \frac{1}{R} \approx \frac{KnWn}{\ell} \left( V_{gs} - V_{th} \right) \] (20)

C. Expression of \(R2\_MOS\) \((V_{gs} = V_{ds})\)

Defining \(\beta = \frac{KnWn}{\ell}\), the relation (16) becomes
\[ I_{ds} = \beta (V_{gs} - V_T) V_{ds} - \frac{1}{2} \beta V_{ds}^2 \] (21)

As drain and gate of the CMOS are connected together, we have
\(V_{gs} = V_{ds}\)
The expression (21) becomes

\[ I_{DS} = \frac{1}{2} \beta V_{DS}^2 - \beta V_T V_{DS} \]  

(22)

The expression of R2_MOS is given by the relation

\[ \frac{1}{R2_{MOS}} = \frac{dV_{DS}}{dV} = \beta(V_{DS} - V_T) = \beta(V_{GS} - V_T) \]  

(23)

\[ R2_{MOS} = \frac{1}{\beta(V_{GS} - V_T)} = \frac{1}{\beta(V_{DS} - V_T)} \]  

(24)

This above 1/R2_MOS conductance is the same as the one given by (20), obtained by approximation of V_{DS}.

We can conclude that since the CMOS transistors use the same drain and gate voltage polarization V_{c1}, this will impose an operation in ohmic zone whatever the values of V_{DS} and V_{GS} are.

D. Study at the locking limit

\[ V_{DS} = V_{GS} = V_T \]

With a CMOS pair there is no ambiguity. When this threshold level is reached for the NMOS, it is not for the PMOS and vice versa.

We have either

\[ V_{c1} - V_c = (V_{GS})_n = (V_T)_{N莫斯} \neq (V_T)_{PMOS} \]  

(25)

or

\[ V_{c1} - V_c = (V_{GS})_n = (V_T)_{PMOS} \neq (V_T)_{N莫斯} \]  

(26)

IV. SIMULATIONS AND RESULTS

The diagrams in Fig.7 and Fig.8 show respectively the shift up and down PLL transient response with a dynamic LPF; Fig.9 and Fig.10 show also respectively the shift up and down PLL transient response but with a fixed LPF. All these diagrams are obtained by simulation with ADS.

![Diagram](image.png)

(a) PLL output frequency shift from 250MHz to 300MHz (b) Charge current (in A) through NMOS for frequency shift up

Fig.7: Transient response of PLL system for a frequency shift from 250 MHz to 300MHz with a dynamic LPF.
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(a) PLL output frequency shift from 300MHz to 270MHz
(b) Discharge current (in A) through PMOS for frequency shift down

Fig.8: Transient response of PLL system for a frequency shift from 300 MHz to 270MHz with a dynamic LPF.

(a) PLL output frequency shift from 250MHz to 300MHz
(b) Charge pump current (in A) for frequency shift up

Fig.9: Transient response of PLL system for a frequency shift from 250 MHz to 300MHz with a fixed LPF.
For each of these above figures, we have at the right side, the PLL charge pump current transient response and at the left side the PLL output frequency transient response.

These results are obtained for a reference frequency $f_{ref}=250$ kHz (so, operate without any stability problem because the cut off frequency is at least lower than the ¼ of reference frequency at the locking state [9]), a divider of the ratio $N$ ($N=N_0+dN$; with the initial ratio $N_0=1000$), a VCO with gain $K_{VCO}=50$ MHz/V and a PFC-IC with gain $K_{PFC}=1$ mA/radian; all the circuit models are from Spice.

From these above simulation results we can notice that during the tracking the perturbation is most important in the case of dynamic LPF as expected and thus, allow a short response time comparing to the one obtained in a fixed LPF.

For example in Fig.7-(a) the PLL output frequency transient response of the CMOS dynamic PLL structure rise up to a maximum value of 450 MHz whereas the one of a fixed resistance PLL structure is 330 MHz, but come back at the expected final frequency value 45µs before the one of the fixed resistance PLL. The same remark can be observe on the charge pump current transient response where there is much dense impulse sourcing or sinking current in a PLL dynamic LPF than in a PLL fixed LPF during a tracking.

The PLL output phase noise responses of Fig.11 give us a maximum value of −113.76 dBc with a fixed LPF and -121.37 dBc with the CMOS dynamic LPF.

Fig.11: PLL system phase noise response in dBC with the dynamic and a fixed LPF.
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The phase noise expressed in dBc here refers to sidebands produced by impulsive noise at the reference frequency and is relative to the main spectrum. It should be noted that our dynamic LPF phase noise performance decrease with the frequency; this can be explained by the additional impedance of parasitic CMOS capacitance with the frequency increasing.

Component values found after optimization: C1=4nF; R1=3.5K; C2=0.5pF; for a fixed LPF, R2=10K.

V. CONCLUSION

We have presented a new model of LPF, the dynamic LPF works like a voltage source when the PLL is locked. Thanks to this behavior, this dynamic LPF reduces considerably the jitters. Its cut-off frequency is approximately 12.66 kHz during locking and 211.3kHz during tracking.

It permits the high frequencies harmonic elimination only during locking and a phase noises level less than -121.37 dBc.

Moreover, it keeps a tracking band-width almost equal to the locking band-width during the tracking, which allows a response time less than 35.4us (time to achieve a 99.41% change).

In this paper, we demonstrate the feasibility of our dynamic LPF. A dedicated technological process and optimizations will give us a customized model for this application and better results, especially with the ultra low threshold voltage CMOS transistors.

REFERENCE